REMARKS

Claims 10-17, 56 and 57 are all the claims pending in the application.

I. Claim Rejections under 35 U.S.C. § 102

Claims 10-12 and 56 were rejected under 35 U.S.C. § 102(b) as being anticipated by Patterson et al. ("Computer Architecture: A Quantitative Approach").

Claim 10, as amended, recites that the execution unit, when the decoding unit decodes an instruction for performing a SIMD operation, the instructions including operands specifying the first register and the second register, refers to the flag stored in the flag storage unit, and performs the SIMD operation (i) only on the operand held in the first register when the first flag stored in the flag storage unit indicates a first status even in a case where the operands specify different registers for the first register and the second register. Applicants respectfully submit that Patterson does not disclose or suggest at least this feature of claim 10.

Regarding Patterson, Applicants note that this reference discloses the use of a plurality of different vector instructions (see Fig. B.3 on page B-7). For example, as shown in Fig. B.3, the instruction ADDV is utilized to perform an operation involving operands V1, V2 and V3. In particular, as shown in Fig. B.3, the associated function of ADDV is the adding of elements of V2 and V3, and placing the result of the addition in V1.

In the Office Action, t he Examiner has taken the position that the second register operand of Patterson corresponds to the "flag" of claim 10, and that if the first and second register operands both specify the same register, then an SIMD operation will be executed only on a single register (see Office Action at page 3).

With respect to this position taken by the Examiner, Applicants note that claim 10 has been amended herein to recite that an SIMD operation is performed only on the operand held in the first register when the first flag stored in the flag storage unit indicates a first status even in a case where the operands specify different registers for the first register and the second register.

Thus, even if the second register operand of Patterson is interpreted by the Examiner as corresponding to the "flag" of claim 10, Applicants respectfully submit that if the first and second register operands of Patterson specify different registers, then the SIMD operation in Patterson will clearly be performed on operands held in different registers.

In other words, in Patterson, when the first and second register operands specify different registers, an SIMD operation will not be performed only on the operand held in the first register.

In view of the foregoing, Applicants respectfully submit that Patterson does not disclose, suggest or otherwise render obvious the feature of an execution unit that, when the decoding unit decodes an instruction for performing a SIMD operation, the instructions including operands specifying the first register and the second register, refers to the flag stored in the flag storage unit, and performs the SIMD operation (i) only on the operand held in the first register when the first flag stored in the flag storage unit indicates a first status even in a case where the operands specify different registers for the first register and the second register, as recited in amended claim 10.

Accordingly, Applicants submit that claim 10 is patentable over Patterson, an indication of which is kindly requested. Claims 11, 12 and 56 depend from claim 10 and are therefore considered patentable at least by virtue of their dependency.

In addition, regarding claim 12, Applicants note that this claim recites that the execution unit, when two pieces of data a1 and a2 are stored in the first register and two pieces of data b1 and b2 are stored in the second register, calculates (i) (a1+a1) and (a2+a2) when the first flag indicates the first status, and (ii) (a1+b1) and (a2+b2) when the first flag indicates the second status. In the Office Action, the Examiner has merely pointed to Fig. B-3 of Patterson as allegedly disclosing this feature.

Applicants respectfully disagree with such a position and submit that Fig. B-3 of Patterson does not in any way whatsoever disclose the ability to calculate (i) (a1+a1) and (a2+a2) when the first flag indicates the first status, and (ii) (a1+b1) and (a2+b2) when the first flag indicates the second status. If the Examiner maintains the rejection of claim 12, Applicants kindly request that the Examiner provide a detailed explanation as to how Fig. B-3 of Patterson allegedly discloses such a feature.

III. Claim Rejections under 35 U.S.C. § 103(a)

The Examiner has rejected claims 13-17 and 57 under 35 U.S.C. §103(a) as being unpatentable over Patterson et al. in view of Probin et al. ("Introduction to AltiVec Assembly Language").

Regarding claim 13, Applicants note that this claim recites that the execution unit, when the decoding unit decodes an instruction for performing a SIMD operation, the instruction including operands for specifying the first register and the second register, refers to the flag stored in the flag storage unit, and performs the SIMD operation (i) only on the operand held in

the first register and rounds an operation result when the flag stored in the flag storage unit indicates a first status even in a case where the operands specify different registers for the first register and the second register.

As discussed above with respect to claim 10, in Patterson, even if the Examiner takes the position that the second register operand of Pattereson corresponds to the "flag" of claim 13, Applicants respectfully submit that if the first and second register operands of Patterson specify different registers, then an SIMD operation will not be performed only on the operand held in the first register.

In view of the foregoing, Applicants respectfully submit that Patterson does not disclose or suggest the above-noted feature recited in claim 13. Further, Applicants respectfully submit that Probin does not cure this deficiency of Patterson.

Accordingly, as the combination of Patterson and Probin does not disclose, suggest or otherwise render obvious at least the above-noted feature recited in claim 13, Applicants submit that claim 13 is patentable over the cited prior art, an indication of which is kindly requested. Claims 14, 15 and 57 depend from claim 13 and are therefore considered patentable at least by virtue of their dependency.

Regarding claims 16 and 17, Applicants note that both of these claims depend from claim 10. Applicants submit that Probin fails to cure the deficiencies of Patterson, as discussed above, with respect to claim 10. Accordingly, Applicants submit that claims 16 and 17 are patentable at least by virtue of their dependency.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may best be resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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